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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,464	03/18/2004	Jonathan A. Noquil	90065.001400/.67130.00	5519

7590 10/05/2005

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EXAMINER	
QUACH, TUAN N	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/803,464	NOQUIL ET AL.	
	Examiner	Art Unit	
	Tuan Quach	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 9-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 7-8 are cancelled. New claims 9-15 are added.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 3, 4, are rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi taken with Huang.

Regarding claims 1, 3, 4, Joshi 6,798,044 teaches a multi flip chip module comprising a leadframe 11, an integrated circuit, e.g., die 12, mounted on a first surface of the lead frame 11, a die including a MOSFET 13 flip chip mounted on the other surface of the lead frame, molded body 14 encapsulating the integrated circuit and leaving exposed at least one surface of the MOSFET devices, wherein the exposure permits the joining to a printed circuit board or electrical component board (e.g., column

2 line 52), (e.g., as in claim 3 and 4). That the MOSFET would encompass the power mosfet would have been obvious, e.g., column 1 line 23. Alternatively, such intended use would have been apparent as it would have been obvious to one skilled in the art that the MOSFET device would be capable of such use. See column 1 line 25 to column 3 line 61. Joshi lacks anticipation primarily in that the die pad terminology is not employed and connections using outer leads and bonding wires are not shown.

Huang 2002/0113305 teaches die pad, e.g., 410, for mounting the semiconductor die wherein a lead frame, e.g., 41 correspond to a die pad 410 and leads 411, the die 40 is mounted on die pad 410. See [0047]. The provision of the leads 411 on the lead frame and the bonding wires 42 for connection thereto is also taught, including the connection between bond contacts or bond pads from outer leads to contact areas of the integrated circuit via bonding wires. See [0046] and [0056].

Accordingly, it would have been obvious to one skilled in the art in practicing the above invention to have employed the outer leads and the bonding wires for providing connections since such structures for connection are conventional and advantageous to permit electrical connections to be made to the devices in question. The portion of the lead frame wherein the semiconductor die is mounted corresponds to the die pad as evidenced by Huang; alternatively, such die pad would have been obvious and advantageous for mounting of semiconductor die as evidenced by Huang.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi taken with Huang as applied to claims 1, 3, 4 above, and further in view of Estacio et al and Huang et al.

The references as applied above do not explicitly recite the source bump contacts in the surface of the MOSFETs and the gate bump contacts extending to a corresponding outer lead. Estacio et al. 2003/0189248 teaches the provision of gate bump contacts, e.g., 54, and source bump contacts, e.g., 61/63 for the necessary connections to the device components in question. See the abstract, [0018-0024].

It would have been obvious to one skilled in the art in practicing the above invention to have provided the source bump contacts and gate bump contacts since such correspond to conventional structures enabling connections to the device components as evidenced by Estacio et al. The provision of half-etch die pad would have been conventional and obvious as evidenced by Huang et al. 2001/0001069, [0019] wherein the half-etch metal base would permit the die pad and metal studs to be identified.

Claims 5, 6, 9-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joshi taken with Huang and Woodworth et al.

Re claims 5, 6, 9-15, Joshi 6,798,044 teaches a multi flip chip module comprising a leadframe 11, an integrated circuit, e.g., die 12, mounted on a first surface of the lead frame 11, a die including a MOSFET 13 flip chip mounted on the other surface of the lead frame including peripheral leads 15, second connection bumps 22 thus encompassing ball grid or stud grid joining to the lead frame, molded body 14 encapsulating the integrated circuit and leaving exposed at least one surface of the MOSFET devices, wherein the exposure permits the joining to a printed circuit board or electrical component board (e.g., column 2 line 52), (e.g., as in claim 3 and 4). That the

MOSFET would encompass the power mosfet would have been obvious, e.g., column 1 line 23. Alternatively, such intended use would have been apparent as it would have been obvious to one skilled in the art that the MOSFET device would be capable of such use. See column 1 line 25 to column 3 line 61. Joshi lacks anticipation primarily in that the die pad terminology is not employed and connections using outer leads and bonding wires as in claims 5, 12, 15 or the connection different from ball grid or stud grid and being wirebond as in claims 14 and 15, or the first type of connection as in claim 9, such connection being wire bond as in claim 10, are not shown. The encapsulation using molding insulating resin is notoriously conventional as disclosed above, Joshi, column 2 line 2.

Huang 2002/0113305 teaches die pad, e.g., 410, for mounting the semiconductor die wherein a lead frame, e.g., 41 correspond to a die pad 410 and leads 411, the die 40 is mounted on die pad 410. See [0047]. The provision of the leads 411 on the lead frame and the bonding wires 42 for connection thereto is also taught, including the connection between bond contacts or bond pads from outer leads to contact areas of the integrated circuit via bonding wires. The encapsulation using molding insulating resin is also taught. See [0046] and [0056].

Woodworth et al. 6,476,481 teaches source and gate bumps or electrodes 43 and 44 on the die 22 (column 4 lines 47-65) wherein the frame 35 is patterned to contain external lead conductors, e.g., 25, 27, for connections to the components of the power MOSFET die. The provision of bonding wires source electrodes, is also shown. See column 4 line 58 to column 5 line 20.

Accordingly, it would have been obvious to one skilled in the art in practicing the above invention to have employed the outer leads and the bonding wires for providing connections since such structures for connection are conventional and advantageous to permit electrical connections to be made to the devices in question. The portion of the lead frame wherein the semiconductor die is mounted corresponds to the die pad as evidenced by Huang; alternatively, such die pad would have been obvious and advantageous for mounting of semiconductor die as evidenced by Huang. It would have been conventional and obvious to have provided the source and gate bumps for connection wherein the lead frame is patterned such that connections to leads from the source and gate bump connections can be provided as evidenced by Woodworth et al. The use of a second type of connection as in claim 9, including a type of connection different from ball grid or stud grid as in claim 14, the wirebonds as in claim 12, would have been obvious given the teachings above and the teachings of Woodworth et al. above, wherein such use of wirebonding for contact electrodes would have been further advantageous in order to increase current capacity as evidenced by Woodworth et al. The encapsulation using molding insulating resin, e.g., claim 6, claim 9, 12, 14 last step, is notoriously conventional as disclosed above, Joshi, column 2 line 2, Huang [0046], and as such would have been obvious.

Applicant's arguments filed July 26, 2005 have been fully considered but they are not persuasive.

Applicant argues that Huang and Joshi show the same connection for both dies. Huang 2002/0113305 however teaches die pad, e.g., 410, for mounting the

semiconductor die wherein a lead frame, e.g., 41 correspond to a die pad 410 and leads 411, the die 40 is mounted on die pad 410, e.g., [0047] wherein the provision of the leads 411 on the lead frame and the bonding wires 42 for connection thereto is also taught, including the connection between bond contacts or bond pads from outer leads to contact areas of the integrated circuit via bonding wires. It remains that the use of bonding wires is conventional and advantageous as taught therein, e.g., Huang [0056] wherein such use of bonding wires permit the overall manufacturing process to be cost effective. Furthermore, such use of connection for connecting the terminals of the integrated circuit would have been further obvious and advantageous as evidenced in Woodworth et al. wherein such provision of bonding wires source electrodes is also shown and advantageous to obtain improved current capacity.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Tuan Quach whose telephone number is 571-272-1717. The examiner can normally be reached on M-F from 8:30 AM to 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor Nathan Flynn, can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan Quach
Primary Examiner